EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _

Final Exam

Fall 2020

Due Monday Nov. 23 at 4:15 PM as a .pdf upload on Canvas

Instructions: There are 10 questions and 8 problems. Two points are allocated to each question and the problems are worth 10 points each. Please solve problems in the space provided on this exam, on separate sheets of white unlined paper, or on a tablet pc. When finished, scan or image and upload as a .pdf file in Canvas. Exams are due by 4:15 p.m.

Please show enough of your work on the problems so that the process you followed to obtain a solution is apparent. This will help during grading if partial credit is justified and help verify that the correct solution is obtained for the right reason. Credit will not be given for an answer that may be correct if the solution process is not shown.

Due to the online nature of this exam, students will be expected to adhere to the honor system described in the paragraph and acknowledge adherence with a signature given below. This is an open-book open-notes exam and students can seek basic information using online resources but with the following absolute restrictions. Prior to the Canvas upload due time, no questions or problems should be posted on any electronic forum, no discussions are permitted relating to this exam with anyone else besides the course instructor, and no solutions obtained from any source other than by the student taking the exam are permitted. The course instructor will attempt to respond to questions by email that are sent between 2:00 p.m. and 4:00 p.m.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=350\mu A/V^2$, $\mu_p C_{OX}=70\mu A/V^2$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=8fF/\mu^2$, $\lambda = 0.01V^{-1}$, and $\gamma = 0$. If reference to a bipolar process is made, assume this process has key process parameters for an npn transistor of $J_S=10^{-15}A/\mu^2$, $\beta_n=100$ and $V_{AFn} = \infty$ and those for a pnp transistor are $J_S=10^{-15}A/\mu^2$, $\beta_p=20$ and $V_{AFp} = \infty$. If any other process parameters are needed, use the process parameters associated with the process described in the attachments to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters.

Even though this is an open-book open-notes exam, several tables that may be of use are appended at the end of the exam should they be of use to you.

Honor System Adherence Signature:

I certify that I have adhered to the honor system policy described in the second paragraph above _____

1. (2 pts) What region of operation in the BJT corresponds to the saturation region of operation in the MOSFET

2. (2pts) If processing equipment with the same resolution is used to form MOS transistors and BJTs, how does the area of a minimum-sized BJT compare to the area of a minimum-sized MOSFET (check 1)

   ☐ Areas about the same

   ☐ Area of BJT about 10 times larger than MOS device

   ☐ Area of BJT about 20 times larger than MOS device

3. (2 pts) What is the major reason CMOS technology replaced depletion mode p-channel MOS technology in the design of digital integrated circuits

4. (2 pts) Two-port models are widely used to model devices and to model circuits and subcircuits. Two widely used models are the y-parameter model (y_{11},y_{12},y_{21},y_{22}) and the amplifier parameter model (R_{IN}, A_V, A_{VR}, R_{OUT}). Assume a transistor is used as part of the design of a voltage amplifier. Check one of the following:

   ☐ The y-parameter two-port model of the transistor will give more accurate results for analyzing the amplifier

   ☐ The amplifier parameter two-port model of the transistor will give more accurate results for analyzing the amplifier

   ☐ The accuracy with using the y-parameter model for the transistor will be the same as that using the amplifier-parameter model for the transistor

5. (2 pts) In your basic circuits course (EE 201 here at ISU) there were four basic dependent sources. One of these was the voltage dependent voltage source. Give the two-port model of the voltage dependent voltage source in terms of the four amplifier parameters {R_{IN}, A_V, A_{VR}, R_{OUT}}.

6. (2 pts) In the analog and digital integrated circuits discussed in this course, circuits were built with resistors, capacitors, and transistors. What is the major reason inductors were not used?

7. (2 pts) The common source (CS) amplifier with an ideal current source bias and the common emitter (CE) amplifier with an ideal current source bias both have voltage gains that can be expressed in terms of the small signal model parameters as $A_v = -\frac{g_m}{g_0}$ yet the numerical value for the magnitude of the gain of the CE amplifier was much larger than that of the CS amplifier. What is the major reason that the numerical value of the gain of the CE amp is much larger than that of the CS amplifier?

8. (2 pts) Dynamic logic is somewhat more complicated than static CMOS or ratio logic yet there can be a significant benefit from using dynamic logic in some applications. What is the major advantage dynamic logic offers in some applications?

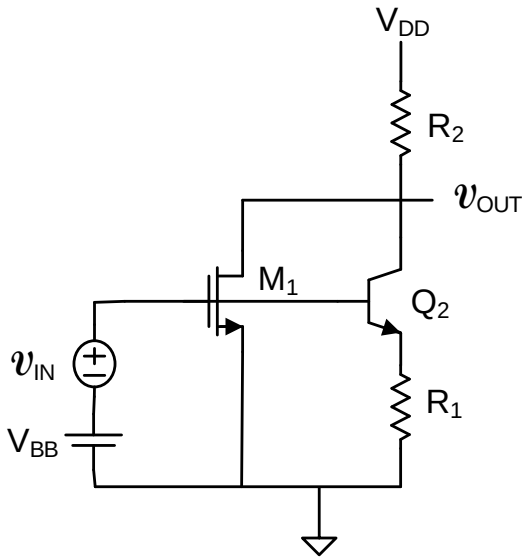
9. (2 pts) If a 6-input NOR gate is to be sized for equal worst-case rise and fall times and if the OD=8, what are the dimensions of the p-channel transistors?

10. (2 pts) The gate-drain overlap capacitance density is given in the process description appended to this exam but the lateral diffusion (L_D) is not given. What is L_D for this process?

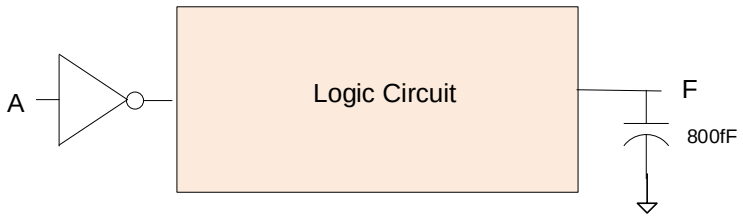
Problem 1 (10 pts) Assume the yield of a die of area A in a particular process with a defect density of d_1 is 50%. If the process engineers are able to reduce the defect density by 10%, what would be the yield?

Problem 2 (10 pts) In the following circuit, assume transistor M_1 is operating in the saturation region and Q_2 in the forward active region.

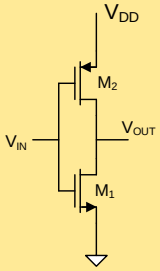
a) Draw the small-signal equivalent circuit
b) Determine the voltage gain in terms of the small-signal model parameters
c) Determine the input impedance in terms of the small-signal model parameters



Problem 3 (10 pts) Consider a Boolean signal A that is at the input to a reference inverter. Design a Logic Circuit that can drive an 800fF load at the output F with a propagation delay from A to F that satisfies the expression $45t_{REF}<t_{PROP}<55t_{REF}$ with the static Boolean expression F = A. You can use at most 10 levels of logic. Give device dimensions on all devices in your design. Assume the characteristics of a reference inverter for this process shown below.



Reference Inverter



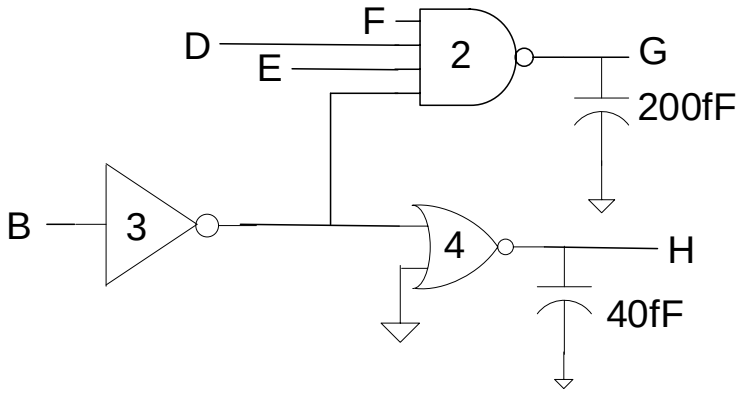
V_{DD}=4.5V μ_n/μ_p=3
V_{TH}=0.5V
$\mu_n C_{OX}$=100fF/μ^2
$W_n=W_{MIN}$ $W_p=3W_{MIN}$
$L_n=L_p=L_{MIN}$
$R_{PDREF}=R_{PUREF}$=2.5K
C_{REF}=4fF t_{REF}=20ps

Problem 4 (10 pts) A simple logic circuit designed in a standard CMOS process is shown below along with a reference inverter for this process. Assume the Boolean inputs D, E, and F are all high and that V_{DD}=4.5V.

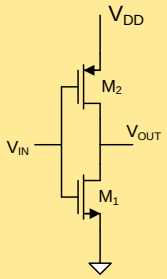
a) If the B input signal is a 500 MHz square wave, determine the dynamic power dissipation in the inverter.

b) Determine the dynamic power dissipation in the 4-input NAND gate.

c) Repeat part B is all devices are minimum sized

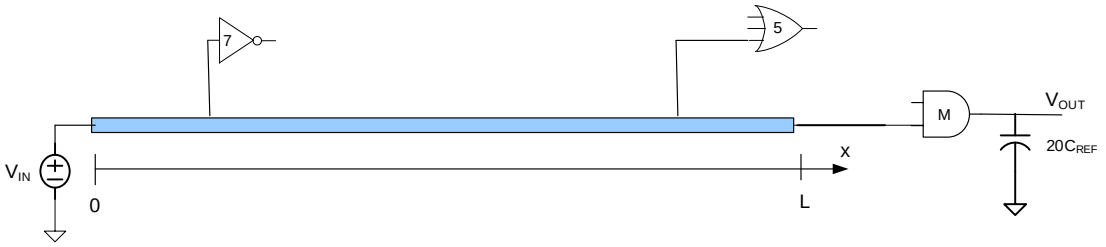


Reference Inverter



V_{DD}=4.5V μ_n/μ_p=3
V_{TH}=0.5V
$\mu_n C_{OX}$=100fF/μ^2
$W_n=W_{MIN}$ $W_p=3W_{MIN}$
$L_n=L_p=L_{MIN}$
$R_{PDREF}=R_{PUREF}$=2.5K
C_{REF}=4fF t_{REF}=20ps

Problem 5 (10 pts) Consider a Poly 1 interconnect that is 1mm long and 2µm wide shown in blue below. Device sizing is as indicated. Determine the propagation delay from the input to the output.

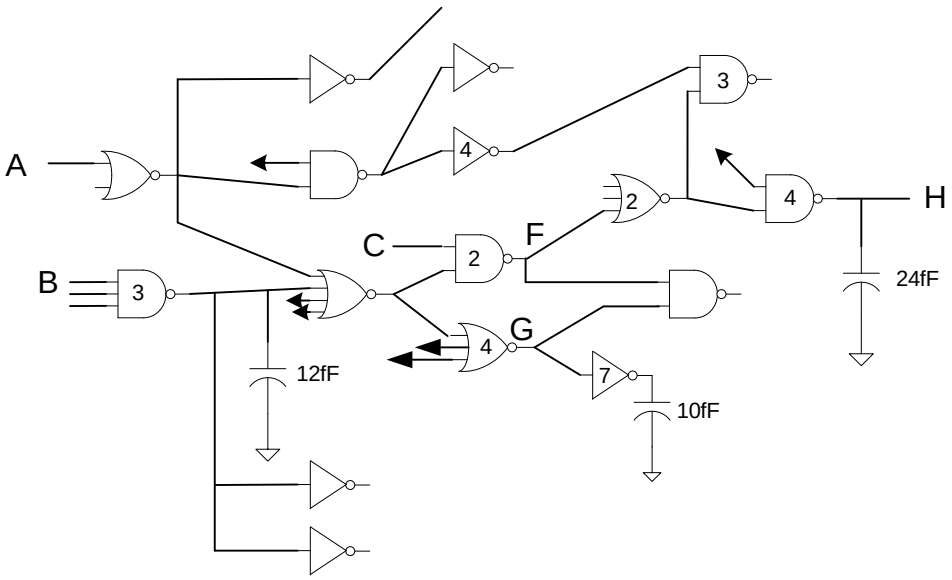


Problem 6 (10 pts) A segment of a logic block is shown below. Assume the lengths of all devices are L_{MIN}. Assume all gates are sized for equal worst-case rise and fall times. Gates with an overdrive factor that is different than 1 are as indicated by a number on the gate. Assume that the process in which these gates are fabricated is characterized by a minimum length reference inverter with

$$t_{REF}=20ps,\ C_{REF}=4fF,\ R_{PDREF}=2.5K$$

a) Determine the worst-case propagation delay from B to G

b) Repeat part a) if all gates are minimum sized.

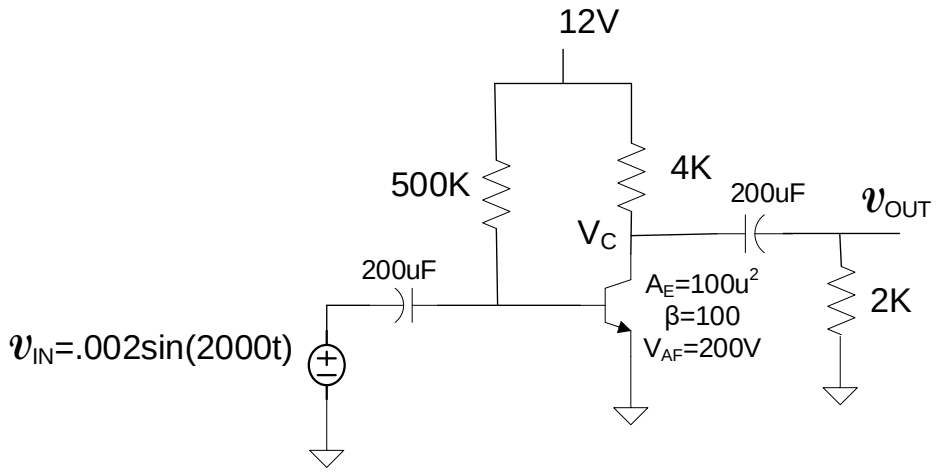


Problem 7 (10 pts) Consider the amplifier shown below.

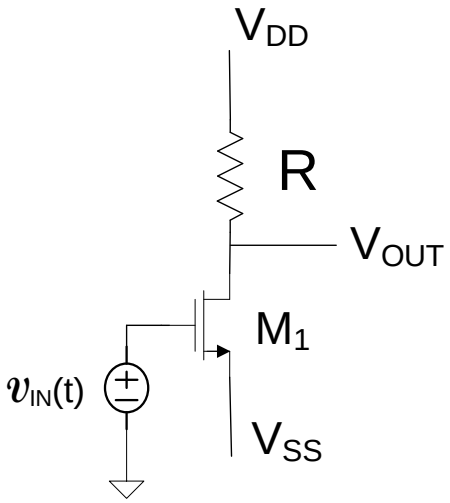
a) Determine the quiescent collector voltage V_C

b) Determine an expression for the small-signal voltage gain $A_V = \frac{v_{OUT}}{v_{IN}}$ in terms of the small-signal model parameters

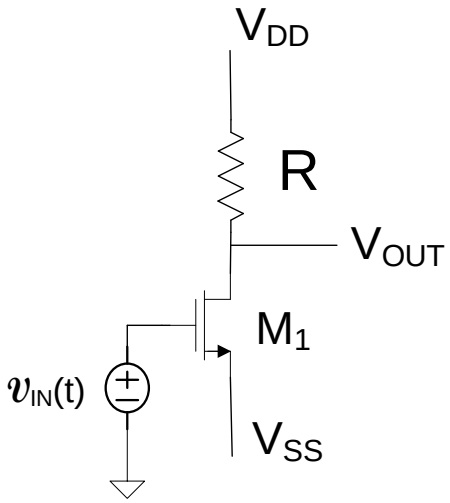
c) Numerically determine an expression for $v_{OUT}(t)$.



Problem 8 (10 pts) Consider the circuit shown below where V_{DD}=2.5V and V_{SS}=-1.5V. Assume you were asked to determine the small-signal voltage gain and have access to the input port and the output port of the amplifier but the only test equipment that you have is a dc volt meter and are allowed to take only one measurement. Further, assume that you do not know the value of R or the dimensions of the transistor M_1 but you were told that the transistor M_1 is fabricated in a process with model parameters μC_{OX}=100uA/V^2, V_{TH}=1V, and λ=0. So you decided to set V_{IN}=0V and measured V_{OUT}=0.5V. What is the small-signal voltage gain?

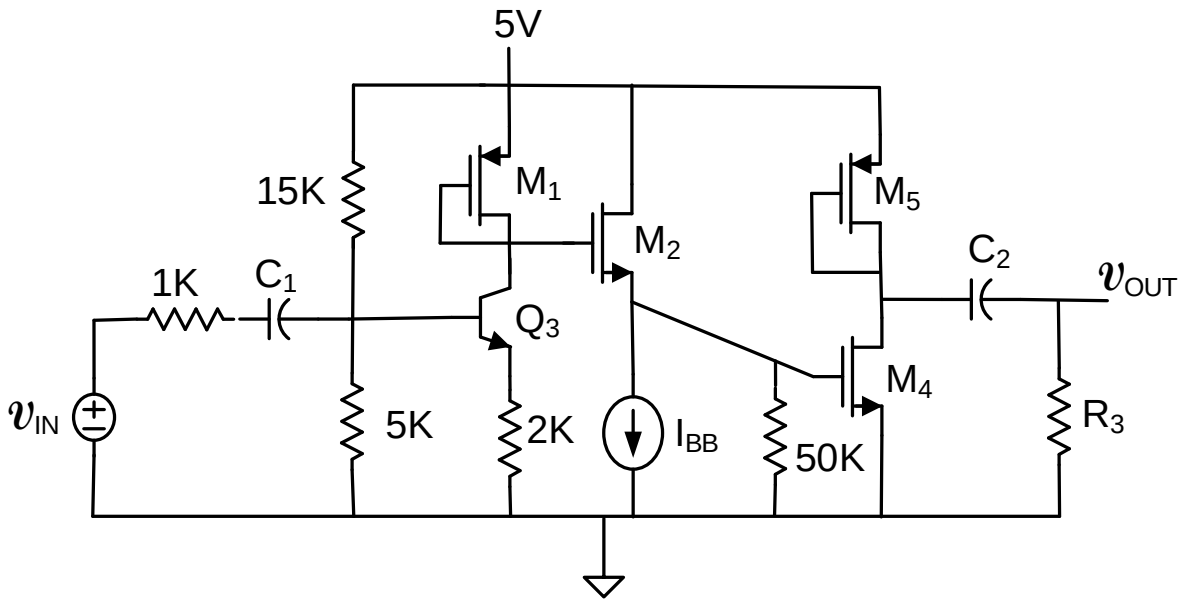


Problem EC Extra Credit (10 pts) Consider the circuit shown below where V_{DD}=2.5V and V_{SS}=-1.5V. Assume you were asked to determine the small-signal voltage gain and have access to the input port and the output port of the amplifier but the only test equipment that you have is a dc volt meter and an AAA battery. Assume you used the dc volt meter to measure the battery voltage and found it measured only 0.1V so you concluded that the battery is exhausted. Further, assume that you do not know the value of R, the dimensions of the transistor M_1, and you do not know any of the transistor model parameters but in this case you are allowed to make 2 measurements. So you decided to set V_{IN}=0V and measured V_{OUT}=0.8V and then you put the exhausted battery at the input (with the positive terminal on the gate) and measured V_{OUT}=0.5V. What is the small-signal voltage gain?



Problem 7 (10 pts) Consider the amplifier block shown below. Assume all MOS transistors are operating in the saturation region and the BJT is operating in the forward active region. Assume the capacitors are all large.

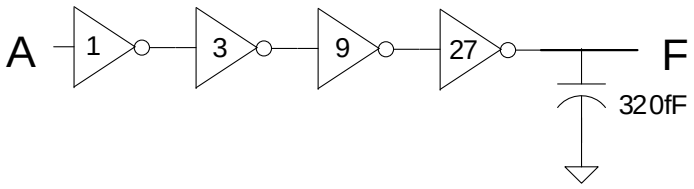
a) Draw the small-signal equivalent circuit of this amplifier
b) Determine the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the components in the circuit
c) Determine the input impedance in terms of the model parameters of the transistors and the components in the circuit



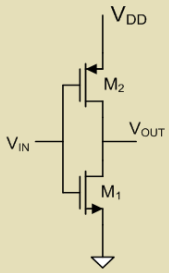
Problem 8 (10 pts) A four-stage pad driver is shown below. The inverters are sized for equal-worst-case rise/fall times with overdrive factors as indicated. A reference inverter for the process is also shown where V_{DD}=3V.

a) Determine the propagation delay of the signal from A to F.

b) Determine the dynamic power dissipation in the third stage (the stage with OD=9) if the input A is a 40MHz 3 Vp-p square wave.



Reference Inverter



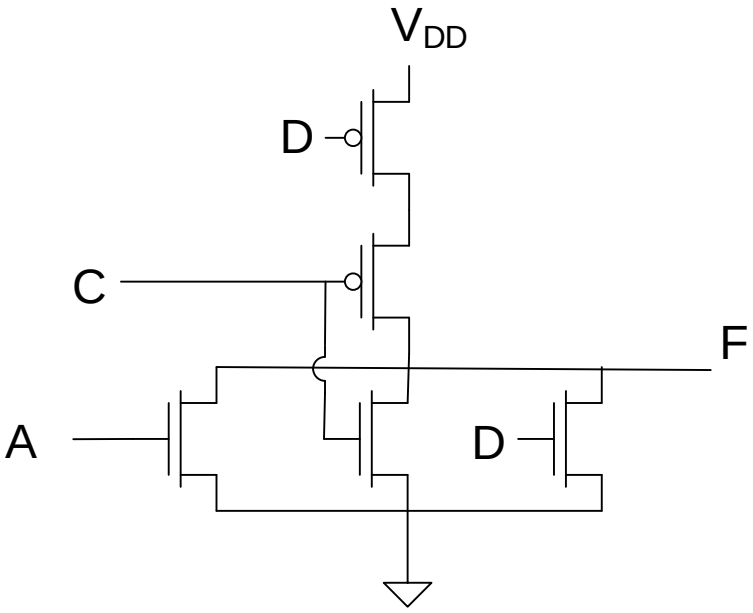
Assume $\mu_n/\mu_p=3$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

$L_n=L_p=L_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

Problem Extra Credit (10 pts – Extra Credit) The following circuit has been proposed as a logic circuit. Will it work? If so, give the truth table. If not, explain why.



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um